IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 7, line 25 is amended as follows:

FIG.2 further shows the generated output PWM waveform 205. The primary period and width write signals are generated as indicated in timing signals P1 and W1 210 and 215, respectively. In some embodiments, the user updates the period value first as indicated in the timing signal 210. Once the user updates the period value, the width value must also be updated as shown in the timing signals 210 and 215. The PWM waveform generator 100 (shown in FIG. 1) can update only the width, which may be necessary in many cases, such as communication related to PWM, where the period value corresponds to a constant sampling period. In these embodiments, updating the width value is what actually transfers the period and width values to their respective secondary period and width registers 120 and 125 from the primary period and width registers 105 and 110 (shown in FIG. 1), respectively, on a next clock cycle as shown in timing signals 230, 235, 220, and 225. The transfer of the period and width values from the primary registers to the secondary registers are based on receiving the secondary storage element write control signal as illustrated using timing signal P2W2 240. The secondary period register 120 actually gets the computed secondary period value (period value – width value). It can be seen in FIG. 2 that the primary period and primary width updates can occur within a PWM signal boundary or can occur across a PWM signal boundary.

The paragraph beginning at page 9, line 9 is amended as follows:

Referring now to FIG. 3, there is illustrated all the timing signals 300, similar to the timing signals shown in FIG.2, generated using the PWM waveform generator 100 shown in FIG.1, according to another embodiment of the present invention. FIG. 3 shows how the present subject matter solves the reliability problem when a sequence of period and width updates/changes, such as PA, PB, and PC 310 and WA, WB, and WC 320 occur on opposite sides of, i.e., occur across, a PWM cycle boundary 330. The generation of the timing signals shown in FIG. 3 clearly illustrate the generation of the PWM waveform without any distortion